REMARKS

This amendment is being submitted in response to the Notice of Non-Compliant Amendment (37 C.F.R. 1.121) dated March 22, 2001. The present amendment includes a clean version of the amended claim(s). Applicants submit that with the exception of the changes made herein regarding the Notice of Non-Compliant Amendment (37 C.F.R. 1.121), the amendment is essentially unchanged with respect to the amendment filed on March 19, 2001.

Claims 1, 2, 3, 4, 5, 6, and 8 have been amended to more clearly define the present invention and the title has been amended to more closely reflect the claimed subject matter. The amendments herein present rejected claim(s) in better form for consideration on appeal. Applicants submit the amendment does not add new matter to the current Application.

Applicants respectfully submit that claim 2 is not indefinite under 35 U.S.C. § 112. Claim 2 has been amended to include a limitation specifying that the copper content of the uppermost interconnect level is at least 90 atomic percent. Support for this limitation can be found on page 7, lines 19-21 of the current specification.

Applicants submit that claim 1 is not anticipated under 35 U.S.C. § 102(b) by U.S. Patent No. 5,149,674 (herein referred to as Freeman). The Office Action states that Applicants have not established a meaning for the term "passivation layer" to exclude a characterization of Freeman's dielectric layer 19. Applicants have accordingly amended claim 1 to further clarify that Applicants' passivation layer is formed over the uppermost interconnect level (which includes an interconnect portion and a bond pad) and more specifically to clarify that the support structures are formed over the *uppermost* surface of the bond pad. This is in contrast to Freeman, which teaches that the structures, formed in dielectric layers 14 and 19 as a consequence of the formation of vias 17 and 22, respectively, are formed *below* the uppermost surface of the bond pad. Freeman teaches that the passivation layer above the uppermost surface of the bond pad includes a single rectangular opening (column 5, lines 30-35). Freeman does not teach a discontinuous opening or multiple openings (either of which would inherently be formed by the presence of the support

structures) and arguably teaches away from the present invention by specifying that only a single opening is formed. Freeman therefore cannot anticipate claim 1.

Applicants believe they have addressed the anticipation rejection with respect to claim 1 and respectfully submit that it is currently distinguishable over Freeman. Applicants further submit that dependent claims 2-6 and 8-11, which depend either directly or indirectly from claim 1, should be allowable for at least those reasons that make claim 1 is allowable.

Applicants, believing that they have addressed the Office Action's rejections, respectfully request allowance of the pending claims or, in the alternative, allowance of the present amendment placing the claims in better form for consideration on appeal. Please feel free to contact me at the number below if there are any issues regarding this amendment or the current Application.

Respectfully submitted,

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VERSION OF CLAIM(S) WITH MARKINGS TO SHOW CHANGES MADE:

1. (Twice Amended) A method of forming a semiconductor device, comprising:

forming an uppermost interconnect level [conductive bond pad] over a semiconductor substrate, wherein the uppermost interconnect level includes an interconnect portion and a bond pad;

forming a passivation layer over the [conductive bond pad] uppermost interconnect level;

removing portions of the passivation layer, wherein removing portions of the passivation layer exposes portions of the bond pad and forms a plurality of support structures [that overlie] overlying the [conductive] uppermost surface of the bond pad [, and wherein removing portions of the passivation layer exposes a portion of the conductive bond pad]; and

forming a conductive capping layer overlying the plurality of support structures, wherein the conductive capping layer electrically contacts [a portion of] the [conductive] bond pad.

2. (Amended) The method of claim 1, wherein a copper content of uppermost interconnect level [the conductive bond pad] is at least 90 atomic percent [comprises mostly copper].

3. (Amended) The method of claim [2] 1, further comprising forming dielectric studs within the [conductive] bond pad, wherein at least a portion of a support structure overlies a portion of a dielectric stud.

4. (Amended) The method of claim 1, wherein the dielectric layer includes a material selected from a group consisting of a [nitride] nitrogen, [and] a hydrogen, and a carbon containing silicon oxide.

5. (Amended) The method of claim 1, wherein the plurality of support structures are interconnected with unremoved portions of the [dielectric] passivation layer.

6. (Amended) The method of claim 5, wherein forming the [conductive bond pad] uppermost interconnect level further comprises forming the [conductive] bond pad over at least one dielectric layer having a Young's modulus less than approximately 50 Giga Pascals.

8. (Amended) The method of claim 1, further comprising forming a barrier layer between the capping layer and the [conductive] bond pad, wherein the barrier layer overlies the support structures and abuts exposed portions of the bond pad excluded by the support structures.